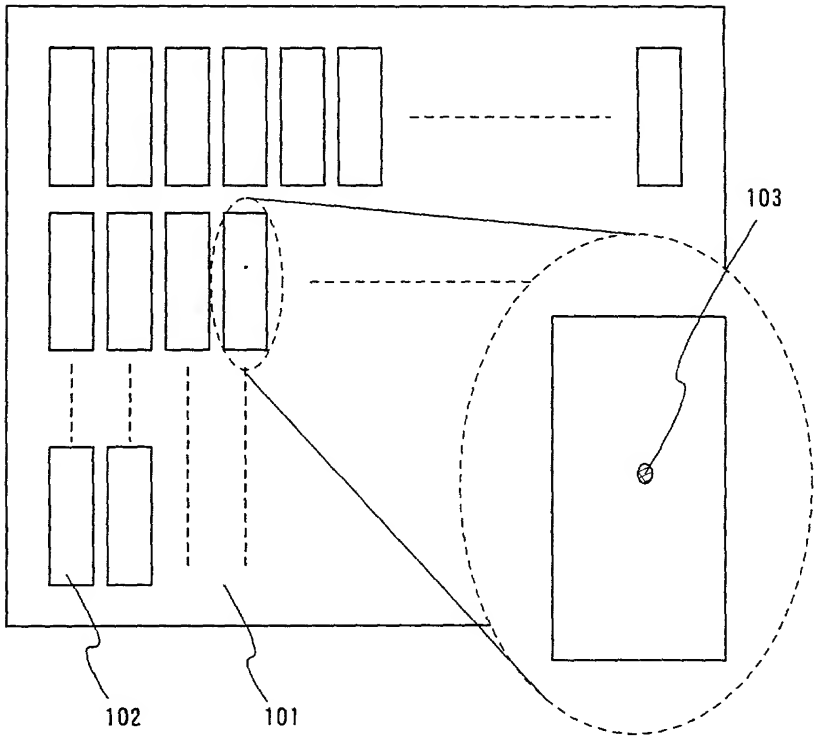


Fig. 1A

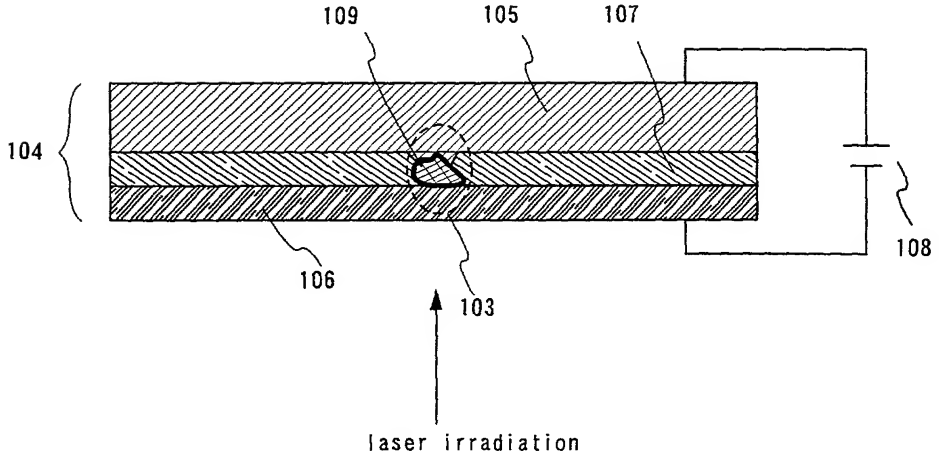


Fig. 1B

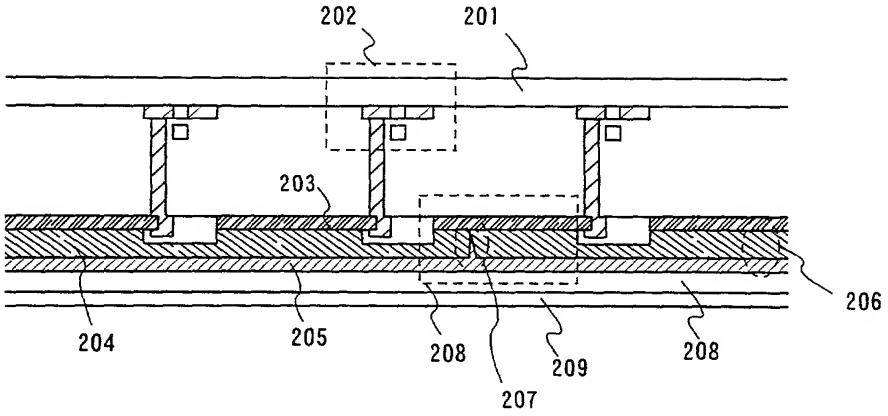

202
201
203
206
204
205
208
209
208
207

Fig. 2A

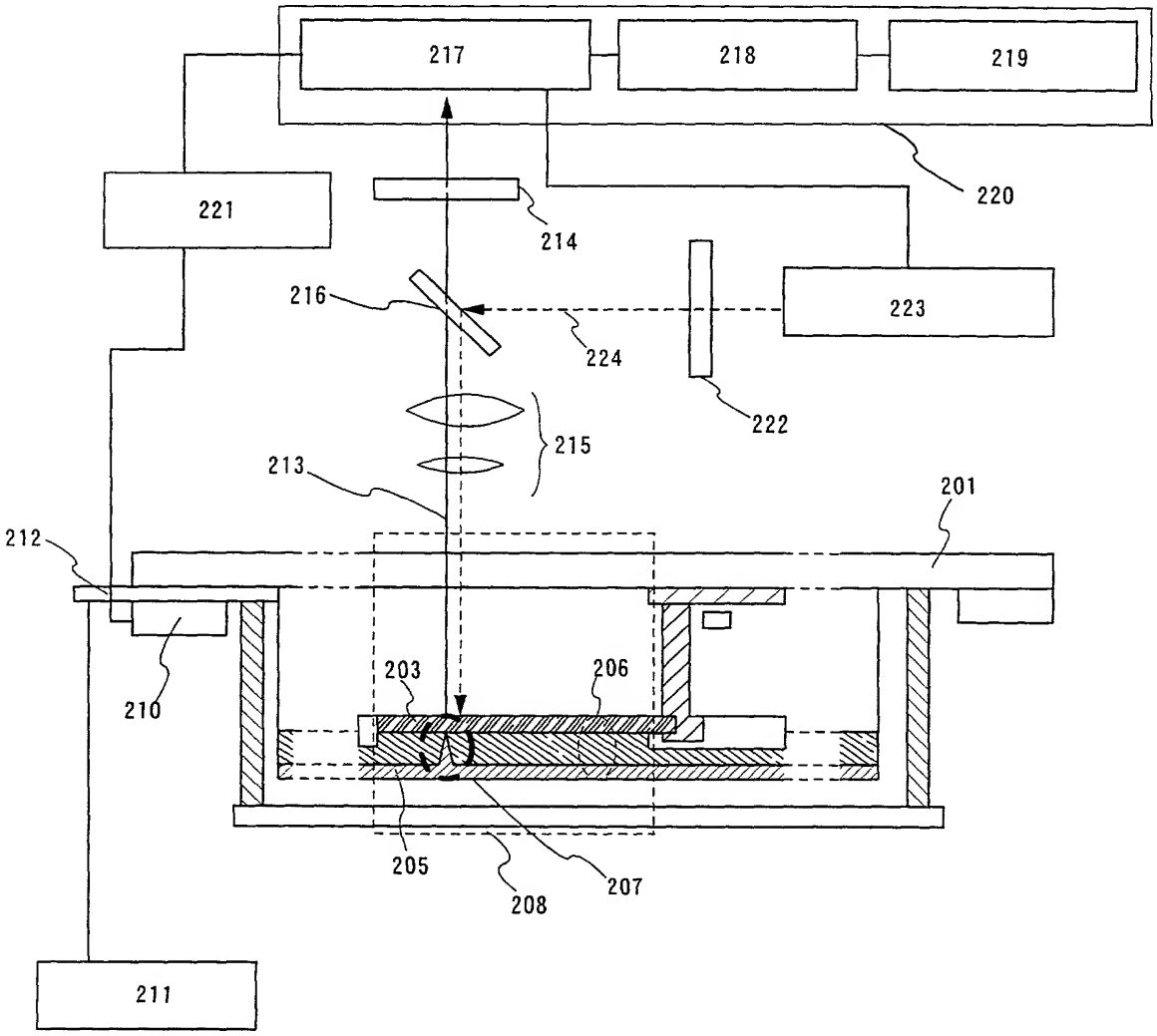

217
218
219
220
221
214
216
223
224
222
215
213
201
212
210
203
206
205
208
207
211

Fig. 2B

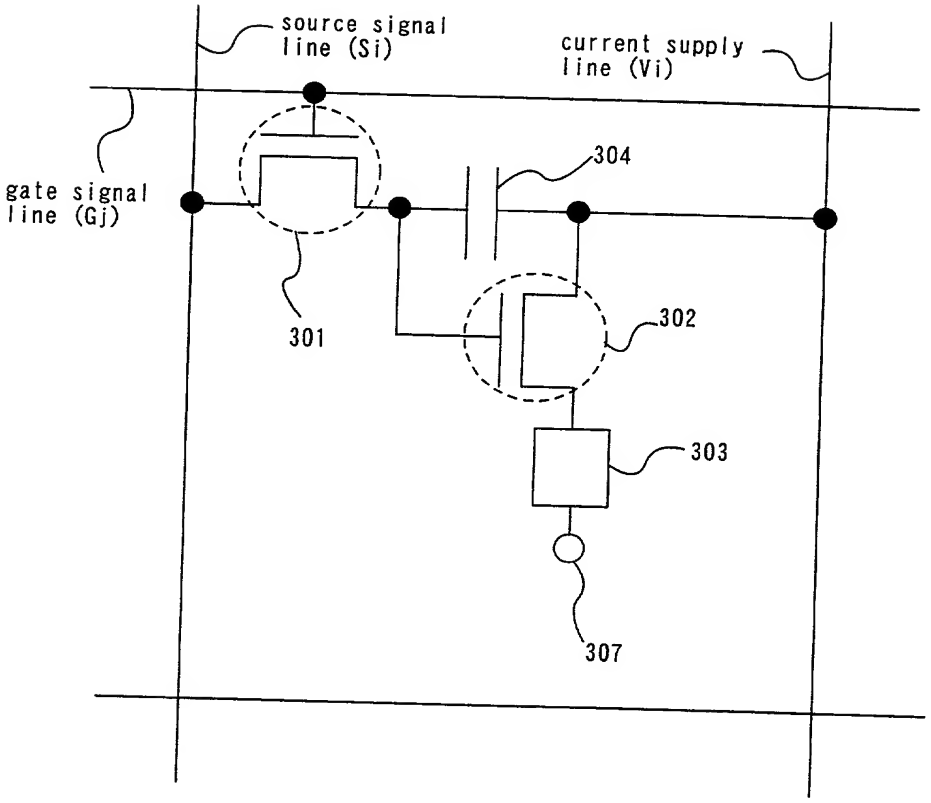

source signal
line (Si)
current supply
line (Vi)
gate signal
line (Gj)
304
301
302
303
307

Fig. 3

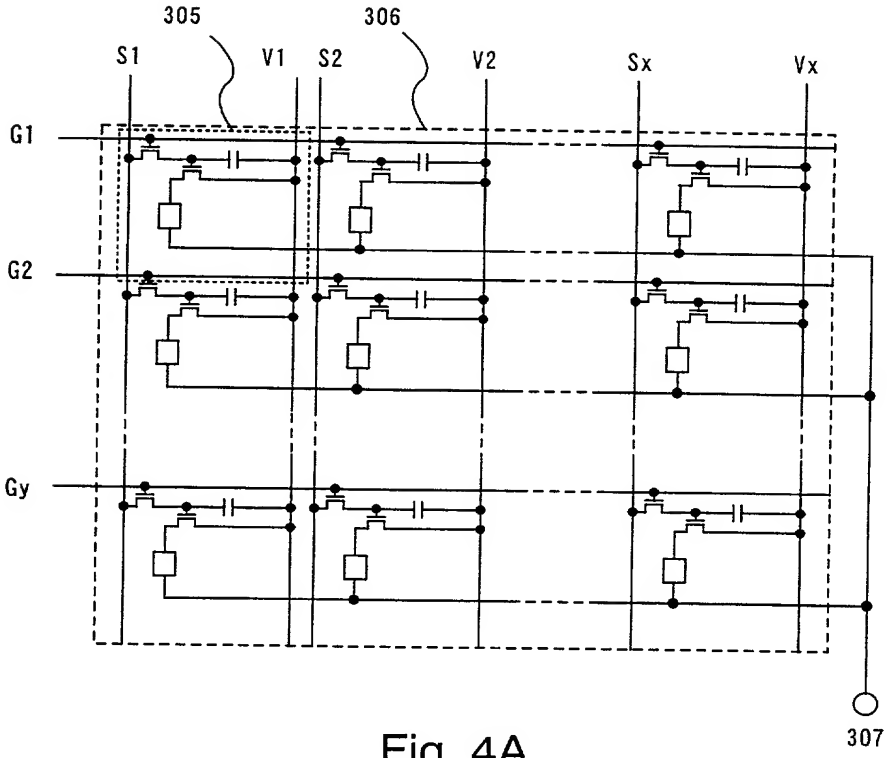

305
306
S1
V1
S2
V2
Sx
Vx
G1
G2
Gy
307

Fig. 4A

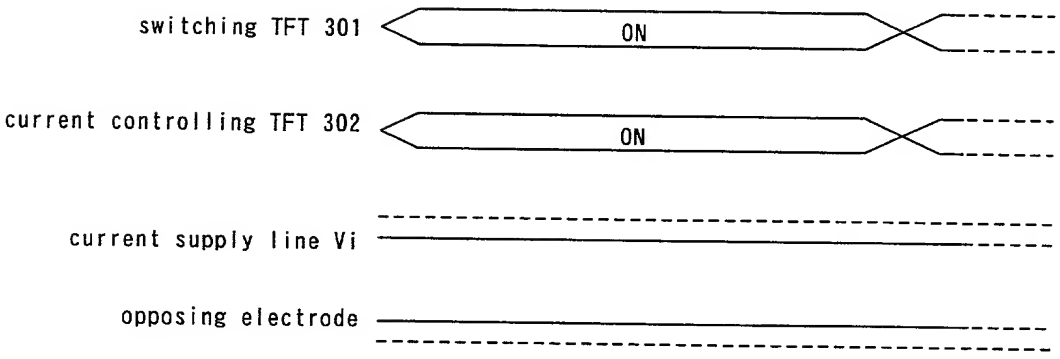
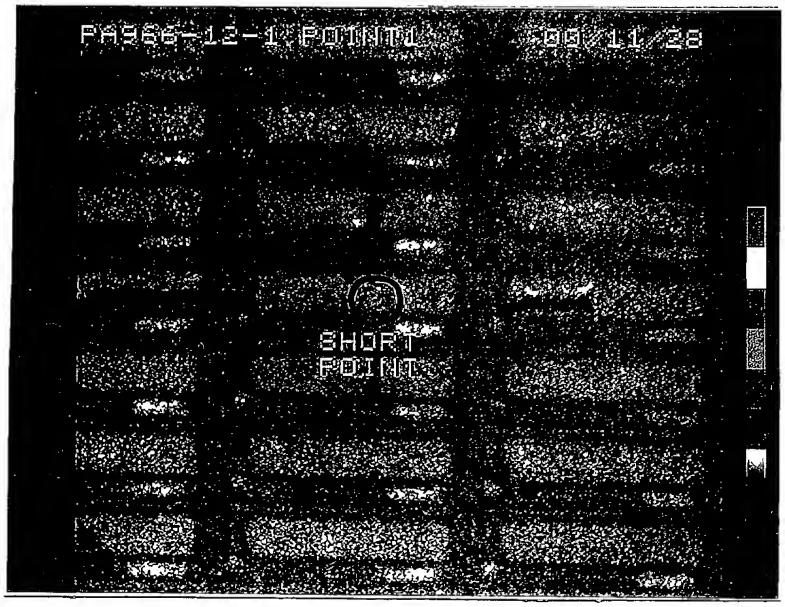
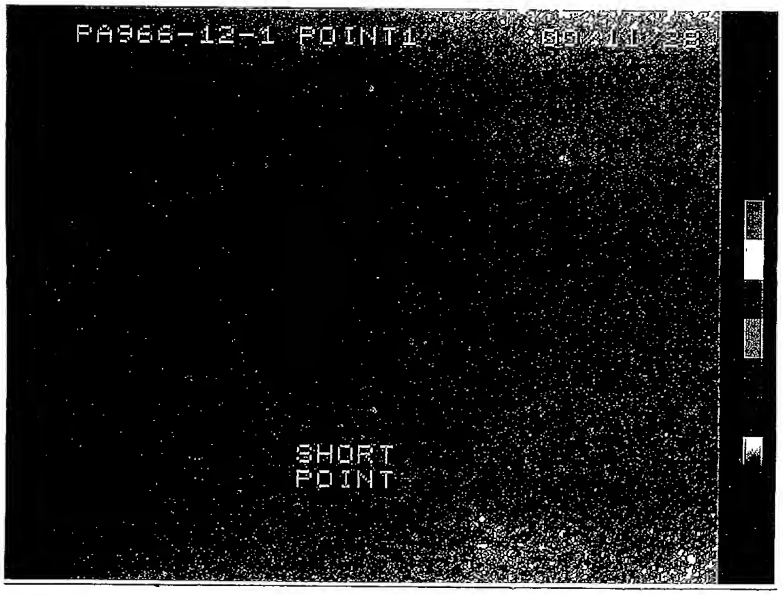

switching TFT 301
ON
current controlling TFT 302
ON
current supply line Vi
opposing electrode

Fig. 4B



×200

Fig. 5A



×500

Fig. 5B

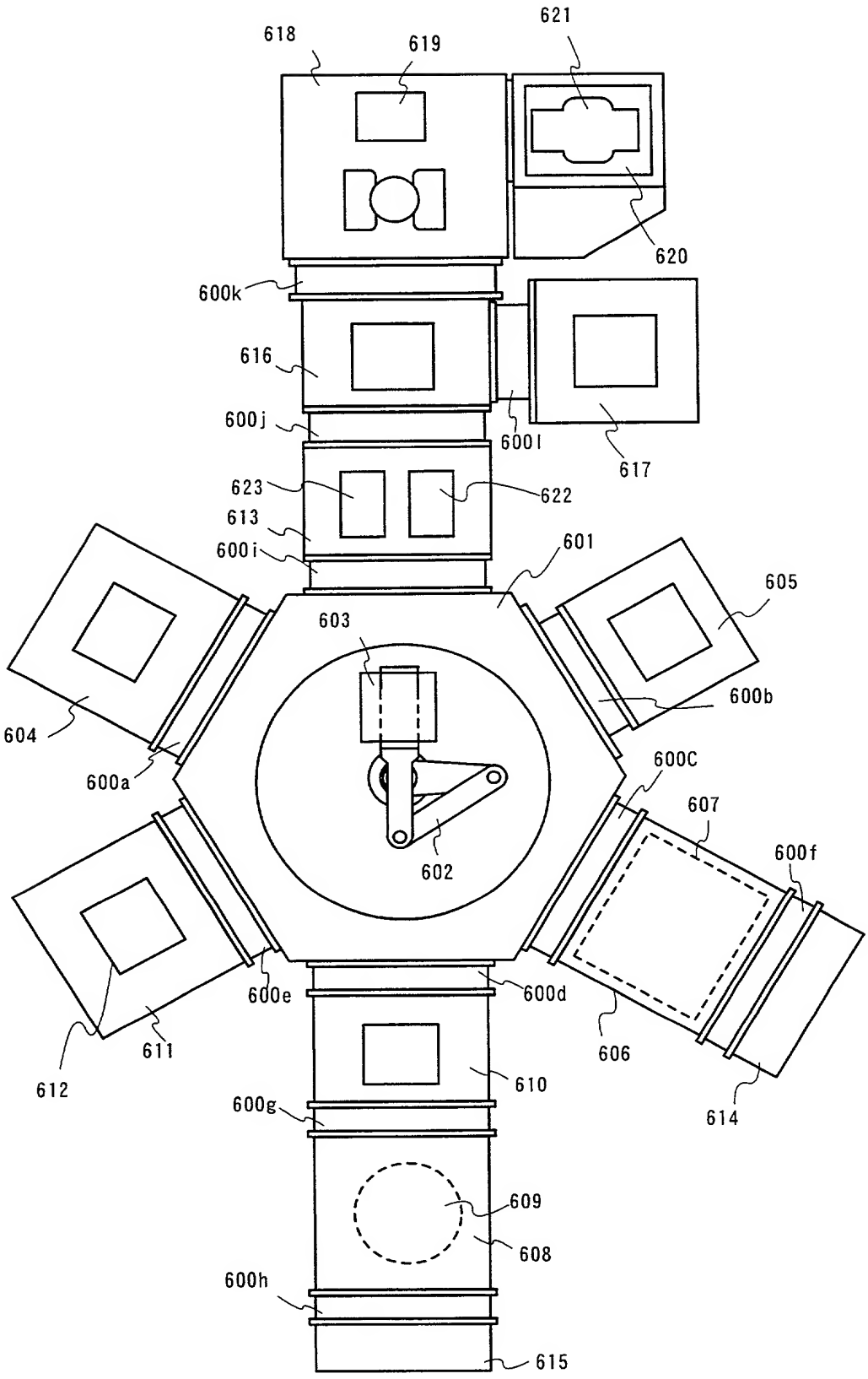

618
619
621
620
600k
616
600j
600l
617
623
622
613
600i
601
605
603
600b
604
600a
600C
607
602
600f
600e
600d
606
611
612
610
614
600g
609
608
600h
615

Fig. 6

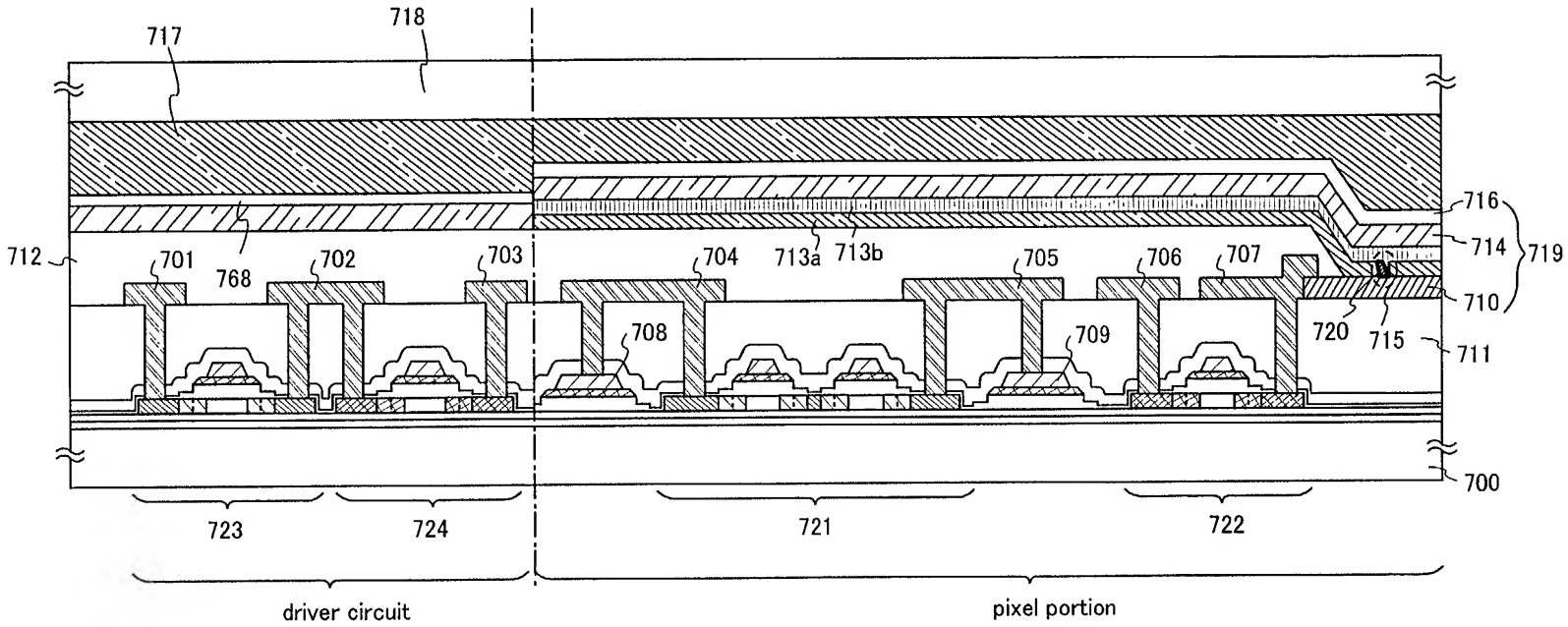
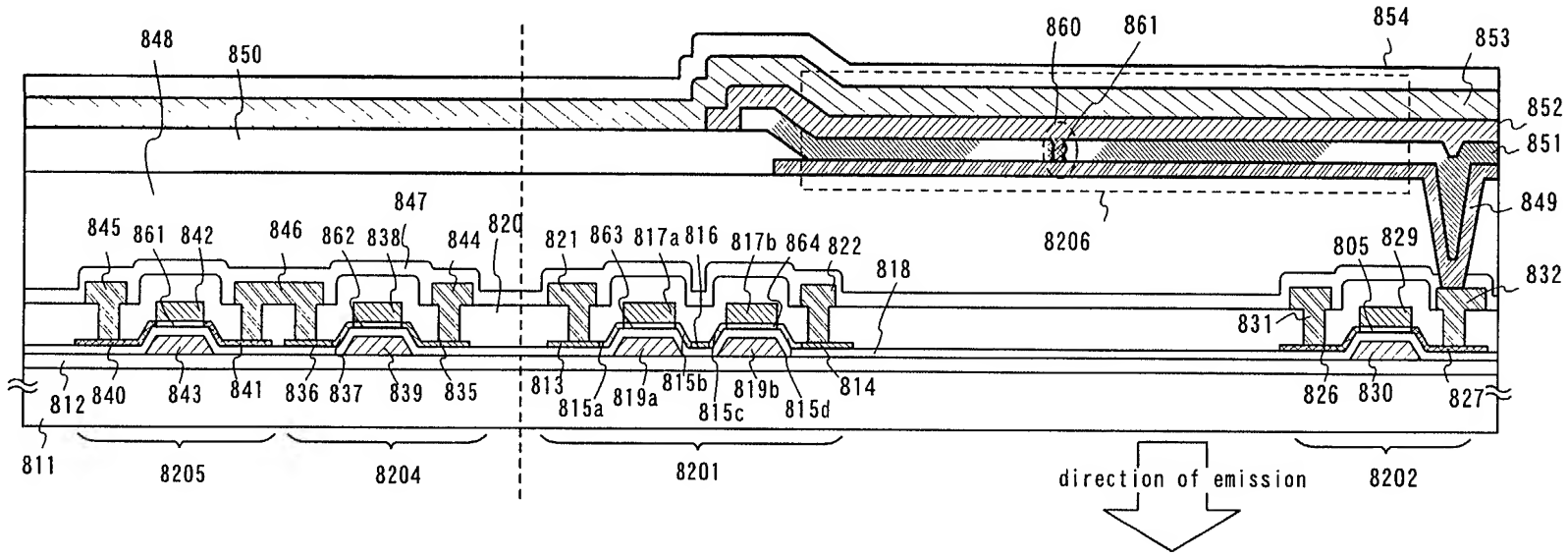

717
718
712
701
768
702
703
704
713a
713b
705
706
707
716
714
719
710
720
715
711
708
709
700
723
724
721
722
driver circuit
pixel portion

Fig. 7



811:substrate 812:base film 813:source region 814:drain region 815a~815d:LDD region 816:separation region
817a, 17b:channel formation region 818:gate insulating film 819a, 819b:gate electrodes 820:first interlayer insulating film
821:source signal line 822:drain wiring 826:source region 827:drain region 828:LDD region 829:channel formation regioin
830:gate electrode 831:source wiring 832:drain wiring 835:source region 836:drain region 837:LDDregion
838:channel formation region 839:gate electrode 840:source region 841:drain region 842:channel formation region
843:gate electrode 844, 845:source wirings 846:drain wiring 847:first passivation film 848:second interlayer insulating film
849:pixel electrode (anode) 850:third interlayer insulating film 851:organic compound layer 852:cathode
853:protecting electrode 854:second passivation film

Fig. 8

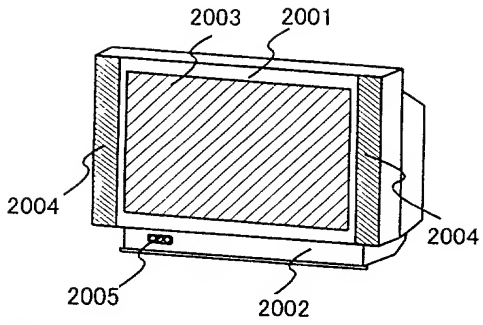


Fig. 9A

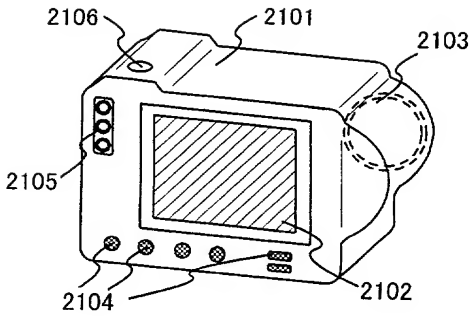


Fig. 9B

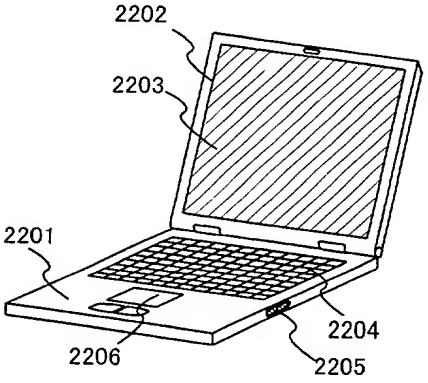


Fig. 9C

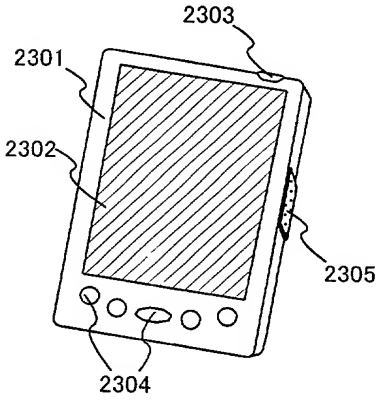


Fig. 9D

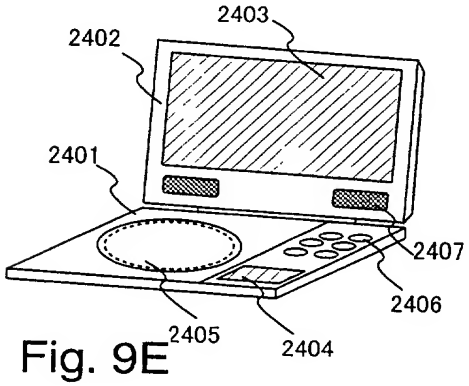


Fig. 9E

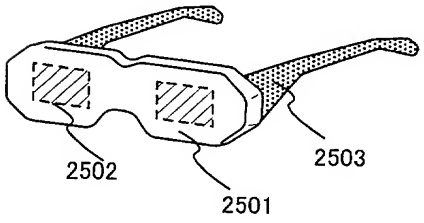


Fig. 9F

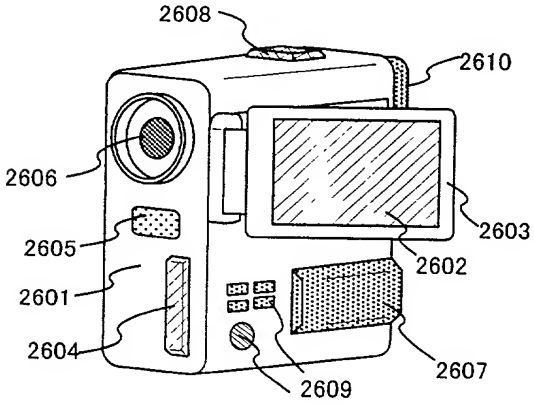


Fig. 9G

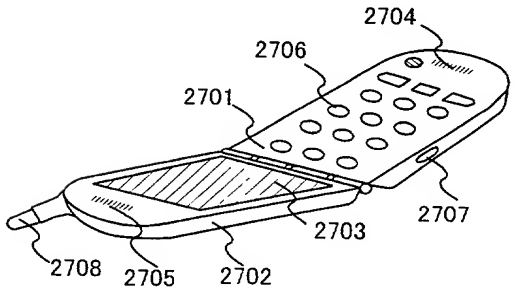


Fig. 9H

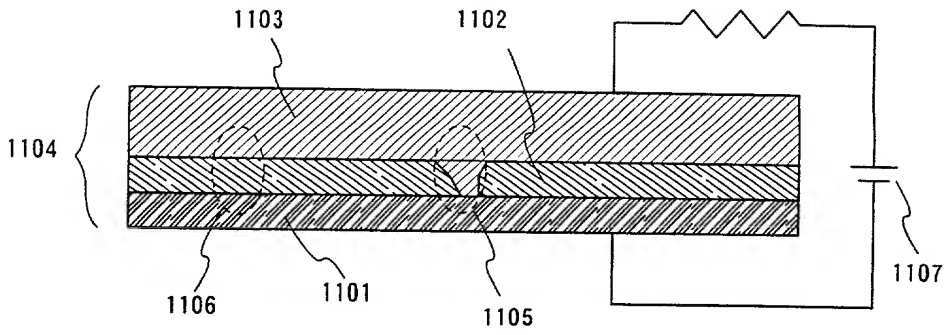


Fig. 10A

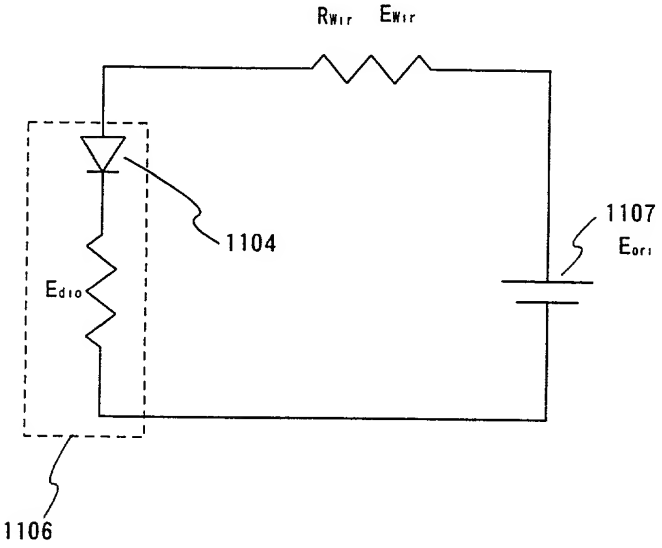


Fig. 10B

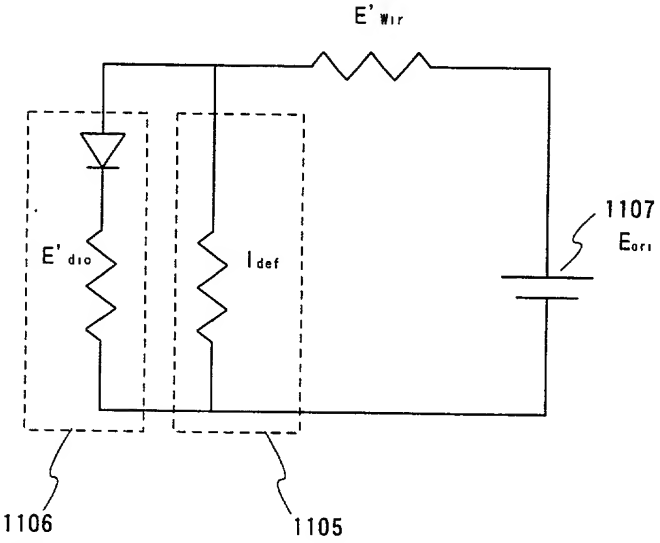


Fig. 10C

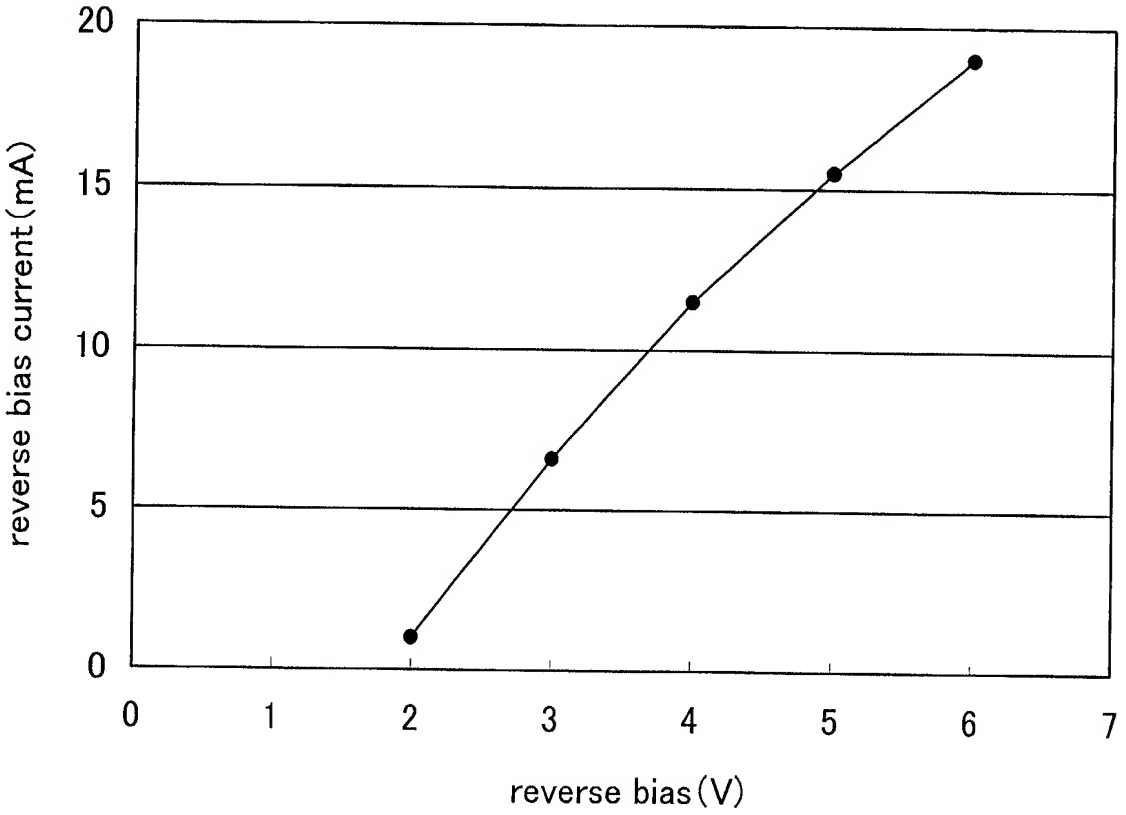


Fig. 11 Current property when a backward bias voltage is applied to a light emitting element